

- quartz
  - crystal, *see* clock
  - window on EPROM, 80
- QuickLogic, 258
- R**
- radian frequency, 274–275
- RAM (random access memory)
  - computer design example, 64
  - defined, 57
  - FPGA, 258, 260–261
- RAS (row address strobe), *see* DRAM
- RC circuit, 272–273
- reactance, *see* capacitor
- recommended operating conditions, 50
- rectifier, *see* diode
- reference designator, 44
- reflection coefficient, *see* transmission line
- refresh, DRAM, *see* DRAM
- register
  - defined, 30
  - within microprocessor, 59
- relative addressing, 74
- reliability testing, 435
- repeater, 114
- reset
  - button debounce, 429
  - computer design example, 67
  - control path logic, 50
  - microprocessor, 62
  - power-on circuit, 132, 428–429
  - vector, 62
- resistor, 267
  - filter, 283–285
  - nonideal model, 277
  - pull-down and pull-up, 298
  - series and parallel combination, 271–272
- return current, *see* signal integrity
- ring network topology, 110–111
- ripple counter, 19–21
- RISC (reduced instruction set computing), 145, 148–149, 162
  - MIPS microprocessor, 148
  - PIC microcontroller, 131
- rising-edge triggered, flip-flop, *see* flip-flop
- ROM (read only memory)
  - computer design example, 64
  - defined, 57
  - full-custom mask, 79
- router, network, 195
- routing, *see* FPGA
- RS-232, 102–107
  - bit-rate generator in 8051, 130
  - breakout box, 104–105
  - DCE/DTE, 104
  - null-modem connection, 104
  - signals, 105
  - versus RS-422, 107
  - voltage levels, 106
- RS-422, 107–108
- RS-485, 112–114
  - distance limitation, 113
  - network design example, 114–117
- RTL HDL design, *see* HDL
- S**
- sampling, 341–344
  - Nyquist frequency, 343, 350–351
- Sanyo, 389
- schematic diagram
  - CAD, 436
  - defined, 6
  - LED driver, 45
  - ripple counter, 20
  - serial receive logic, 49
- Schmitt trigger, 338, 429
- Schottky diode, *see* diode
- scrambling, 200–202
- SDRAM (synchronous DRAM)
  - asynchronous timing requirements, 179
  - auto-precharge (AP), 176
  - back-to-back transactions, 178
  - burst termination, 178
  - CAS latency, 176, 181
  - data mask, 175, 177, 180
  - DDR, 179–182
  - DDR source-synchronous interface, 181
  - internal structure, 174
  - mode register, 177
  - precharge, 175–176
  - read command, 176–177, 181–182
  - refresh, 179
  - row activation, 175
  - synchronous command interface, 174–175
  - write command, 177–178, 182
- search engine, *see* CAM
- segmented memory, 134–136
- selector, *see* multiplexer

- semiconductor, 33, 293
  - junction temperature, 375
- Semtech, 417
- serdes, 199–203
- serial communications
  - computer design example, 64–65
  - defined, 98
  - interrupt handling, 66–67
  - logic design example, 45–50
  - short distance, 118–120
- setup time, flip-flop, *see* flip-flop
- seven-segment display, 43
- shift register
  - defined, 30–31
  - in serial communications, 47
  - JTAG, 431–432
- signal integrity
  - clock distribution, 358–359
  - crosstalk, 408
  - EMC, 413
  - EMI, 410–412
  - reflections, 398–400
  - return current, 402, 410–413
  - transmission line delay threshold, 359
  - transmission line, *see* transmission line
- significantand, floating-point, 165
- silicon, 34
- silicon dioxide, 306
- sine wave, *see* frequency domain analysis
- skin effect, 393
- SMT (surface mount technology), 423
- socket number, 196
- SOIC (small outline integrated circuit), 40
- software
  - address banking, 67–68
  - analogy to finite state machine, 237
  - assembly language, 72–76
  - CAD, *see* CAD
  - CAM management, 189–191
  - defined, 56
  - development tools, 421
  - diagnostic, 433–435
  - handshaking, 100, 104, 107
  - interaction with network hardware, 111
  - interrupt handling, 62–63
  - interrupt instruction, 123, 136
  - interrupt versus polling, 66–67
  - locality and caching, 150–151
  - mask-ROM, 79
  - memory access patterns, 90–91
  - memory aliasing, 65
  - network design example, 117
  - networking, 195
  - page table management, 160
  - subroutine, *see* subroutine
  - virtual memory, 160–161
  - volatile variables and cache, 156
  - watchdog timer operation, 132
- solder
  - breadboard circuit assembly, 425–426
  - reflow assembly process, 423
  - wave assembly process, 423
- source, FET, *see* transistor
- source-synchronous, 181
  - disadvantage, 369
  - timing analysis, 368–369
- SP (stack pointer)
  - defined, 60
  - supervisor and user modes, 139
- SPI (serial peripheral interface), 119–120
- spectrum analyzer, 281
- speculative execution, 164
- Spice, 436–440
  - filter simulation, 437–438
  - transmission line simulation, 438–440
- SRAM (static RAM)
  - asynchronous, 86–88
  - bit structure, 86
  - cache, 150
  - defined, 78
  - linked to CAM, 190
  - performance versus DRAM, 149
  - synchronous, *see* SSRAM
- SSRAM (synchronous SRAM)
  - burst counter, 184
  - DDR burst length, 185
  - DDR interface, 185–187
  - flow-through, 183
  - pipelined, 183
  - QDR, 187–188
  - synchronous interface, 183–184
  - ZBT, 184
- SSI (small-scale integration), 39
- stack
  - defined, 60
  - interrupt, 62
  - push and pop, 60–61
  - usage, 61